IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Ji-Young KIM		
Serial No.:	10/699,047	Examiner:	Duong, Khanh B.
Filed:	October 30, 2003	Group Art Unit:	2822
Confirmation No.:	1200		
For:	MOSFET HAVING RECESSED CHANNEL AND METHOD OF FABRICATING THE SAME		

Date: May 30, 2006

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20060216, dated March 1, 2006, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

1-7. (Cancelled)

8. (Currently amended) A method of forming a MOSFET having a recessed channel, comprising:

forming a trench in a semiconductor substrate;

forming a gate dielectric layer on an inner wall and a bottom of said trench;

sequentially forming a gate conductive layer and a capping layer on the gate dielectric layer so as to fill the trench;

forming a gate electrode having a first portion which rises over the semiconductor substrate and a second portion filling the trench by simultaneously patterning the capping layer and the gate conductive layer, wherein the first portion has a smaller width than that of the second portion; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode.

9. (Previously presented) The method of claim 8, wherein forming the trench comprises:

forming a rectangular trench in the semiconductor substrate using an etch process; and

making the trench have a round profile by further etching the trench using a chemical dry etch process.

10. (Previously presented) The method of claim 9, wherein the rectangular trench is formed to a depth of about 1000Å to 1500Å and is further etched by about 100Å to about 200Å using a chemical dry etch process.

11. (Previously presented) The method of claim 8, wherein the gate dielectric layer is formed of one selected from the group consisting of a silicon oxide layer, a titanium oxide layer, and a tantalum oxide layer.

12. (Previously presented) The method of claim 8, wherein the gate conductive layer comprises a conductive polysilicon layer that fills the trench and a metal layer formed on the conductive polysilicon layer.

13. (Previously presented) The method of claim 8, wherein forming the trench further compromises:

forming a sacrificial oxide layer by thermally oxidizing the semiconductor substrate; and

removing the sacrificial oxide layer using a wet etch process.

14. (Previously presented) The method of claim 8, wherein forming the gate electrode comprises recessing the gate conductive layer that fills the trench to a depth of 500Å or less from the surface of the semiconductor substrate

15. (Previously presented) The method of claim 8, further comprising forming spacers on sidewalls of the gate electrode.

16 Cancelled

17. (Previously presented) The method of claim 14, further comprising forming spacers on the sidewalls of the gate electrode, wherein a portion of the spacers are extended into the semiconductor substrate.

18. (Previously presented) The method of claim 9, wherein the etch process is a reactive ion beam etch process.

19. (Previously presented) The method of claim 8, wherein the source/drain region is shallower than the bottom of the trench.

20. (Currently amended) A method of forming a MOSFET having a recessed channel, comprising:

forming a trench in a semiconductor substrate using a etch process;

forming a gate dielectric layer on an inner wall and a bottom of said trench;

sequentially forming a gate conductive layer and a capping layer on the gate dielectric layer so as to fill the trench;

forming a gate electrode having a first portion which rises over the semiconductor substrate and a second portion filling the trench by simultaneously patterning the capping layer and the gate conductive layer, wherein the first portion has a smaller width than that of the second portion;

forming spacers on the sidewalls of the gate electrode, wherein a portion of the spacers are extended into the semiconductor substrate; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode,

and wherein forming the gate electrode comprises recessing the gate conductive layer that fills the trench to a depth of 500Å or less from a top surface of the semiconductor substrate by adjusting etching time.

21. (Previously presented) The method of claim 20, wherein the trench is formed to a depth of about 1000Å to about 1500Å and is further etched by about 100Å to about 200Å using a chemical dry etch process.

22. (Previously presented) The method of claim 20, wherein the source/drain region is shallower than the bottom of the trench.

23. (Previously presented) The method of claim 15, wherein the width of the first portion of the gate electrode plus the spacers is less than that of the second portion of the gate electrode.

24. (Previously presented) The method of claim 23, wherein the spacers extend the entire height of the first portion of the gate electrode.

25. (New) A method of forming a semiconductor device having a recessed channel, comprising:

forming a rectangular trench in a semiconductor substrate using an etch process;

forming a gate dielectric layer on an inner wall and a bottom of said trench;

forming a gate conductive layer and a capping layer on the gate dielectric layer to fill the trench;

forming a gate electrode having a first portion which rises over the semiconductor substrate and a second portion filling the trench by simultaneously patterning the capping layer and the gate conductive layer, wherein the first portion has a smaller width than that of the second portion, and wherein forming the gate electrode comprises recessing the gate conductive layer that fills the trench to a depth of 500Å or less from the surface of the semiconductor substrate; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode.

26. (New) The method of claim 25, wherein forming the capping layer is performed immediately after forming the gate conductive layer.